EE 330
Lecture 17

MOSFET Modeling

Exam Schedule

Exam 1	Friday Sept 24
Exam 2	Friday Oct 22
Exam 3	Friday Nov 19
Final	Tues Dec 14 12:00 p.m.

Prelab Annuncement

A Pre-Lab will be posted on Canvas for Lab 2

Photo courtesy of the director of the National Institute of Health (NIH)
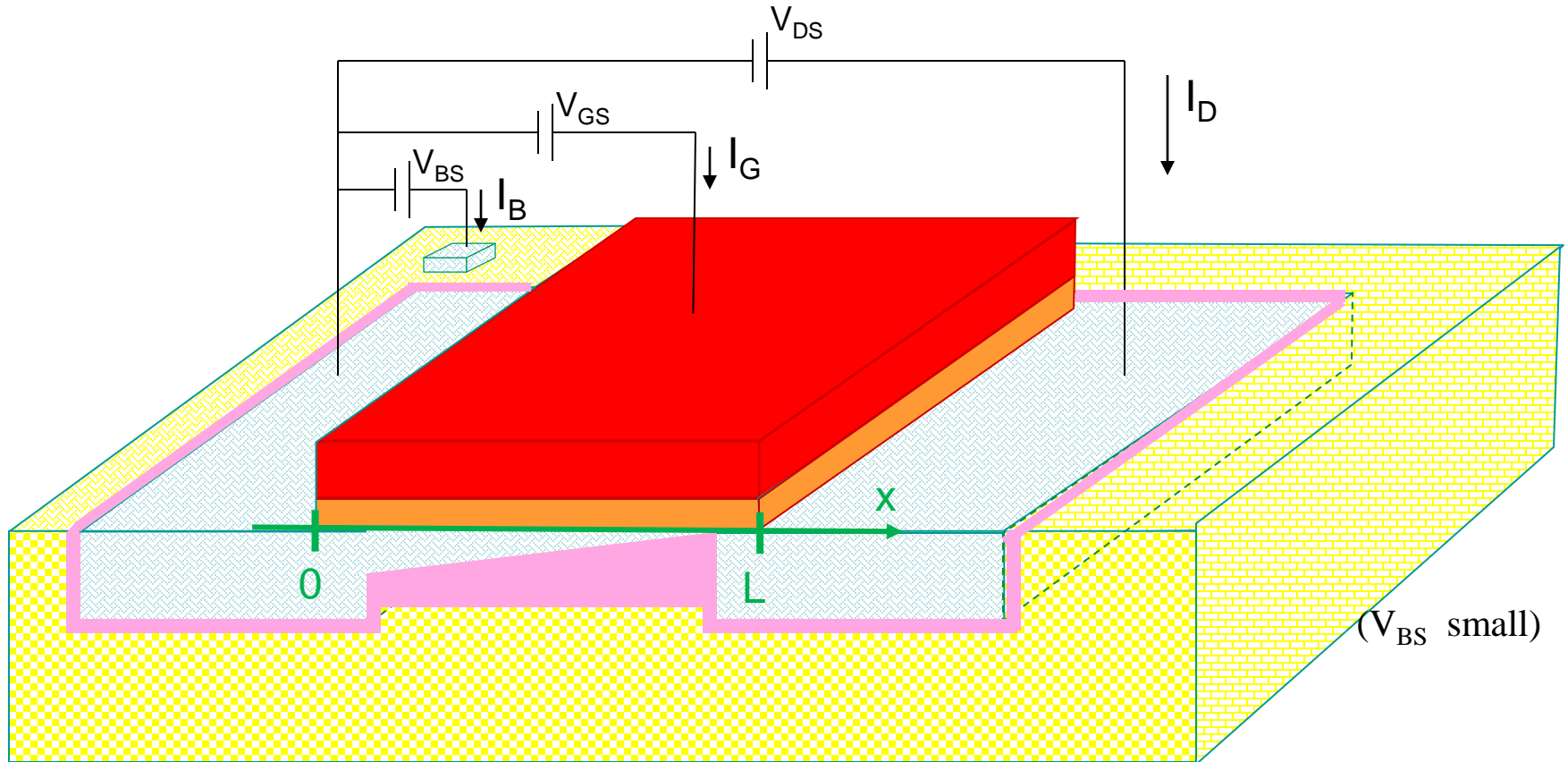
Masks Save Lives

NIH

As a courtesy to fellow classmates, TAs, and the instructor

Wearing of masks during lectures and in the laboratories for this course would be appreciated irrespective of vaccination status

n-Channel MOSFET Operation and Model

Increase V_{DS} even more (beyond $V_{GS}-V_{TH}$)

Nothing much changes !!
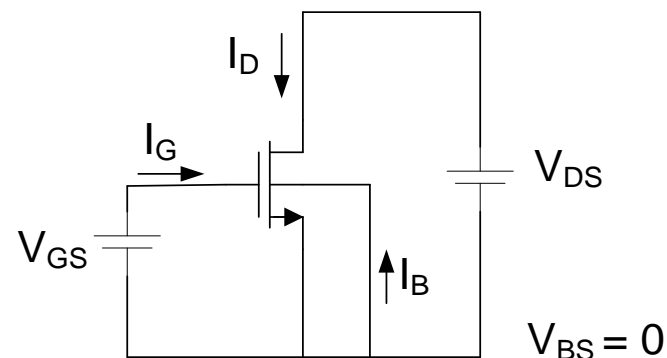
Termed "saturation" region of operation

I_D=?

I_G=0

I_B=0

Model Summary
n-channel MOSFET

$$I_D = \begin{cases} 0 & V_{GS} \leq V_T & \text{Cutoff} \\[3mm] \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_T - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T & \text{Triode} \\[5mm] \mu C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_T\right)^2 & V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T & \text{Saturation} \end{cases}$$

$I_G = I_B = 0$

Model Parameters: {μ, V_T, C_{OX}} Design Parameters : {W, L}
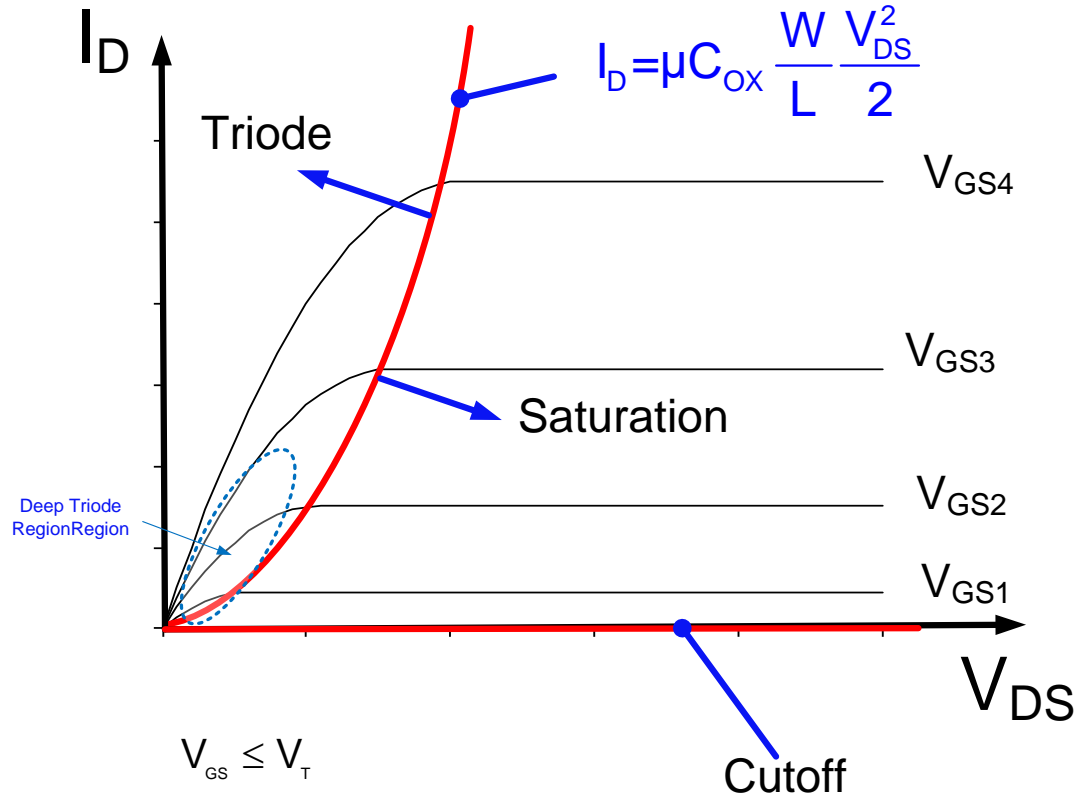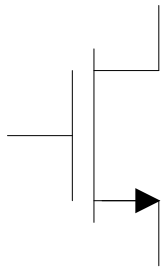
This is a piecewise model (not piecewise linear though)

This piecewise model is continuous at transitions between regions

(Deep triode special case of triode where V_{DS} is small $R_{CH} = \dfrac{L}{W}\dfrac{1}{(V_{GS} - V_T)\mu C_{OX}}$)

Note: This is the third model we have introduced for the MOSFET

Graphical Representation of MOS Model

$$I_D = \mu C_{OX} \frac{W}{L} \frac{V_{DS}^2}{2}$$

Triode

V_{GS4}

Saturation

V_{GS3}

Deep Triode
RegionRegion

V_{GS2}

V_{GS1}

Cutoff

$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{OX} \dfrac{W}{L} \left(V_{GS} - V_T - \dfrac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{OX} \dfrac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T \end{cases}$$
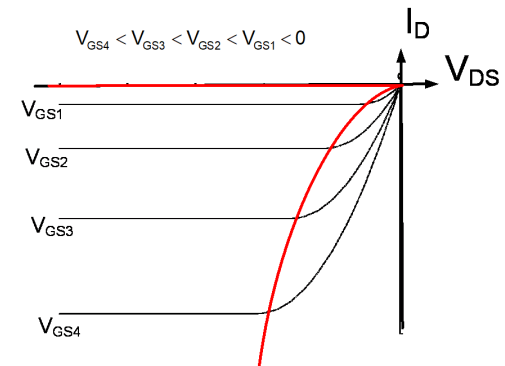
$$I_G = I_B = 0$$
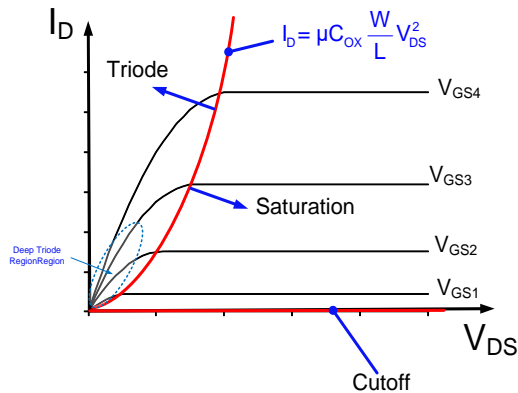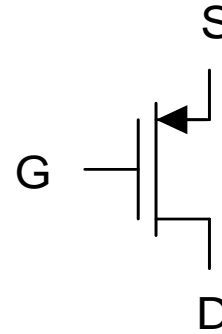
Parabola separated triode and saturation regions and corresponds to $V_{DS} = V_{GS} - V_T$

PMOS and NMOS Models
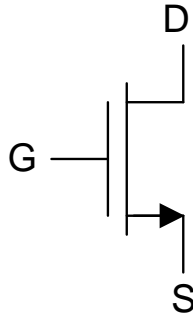
- Functional form identical, sign changes and parameter values different
- Will give details about p-channel model later

Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T = 1V$ and $\mu C_{OX} = 100 \mu A V^{-2}$
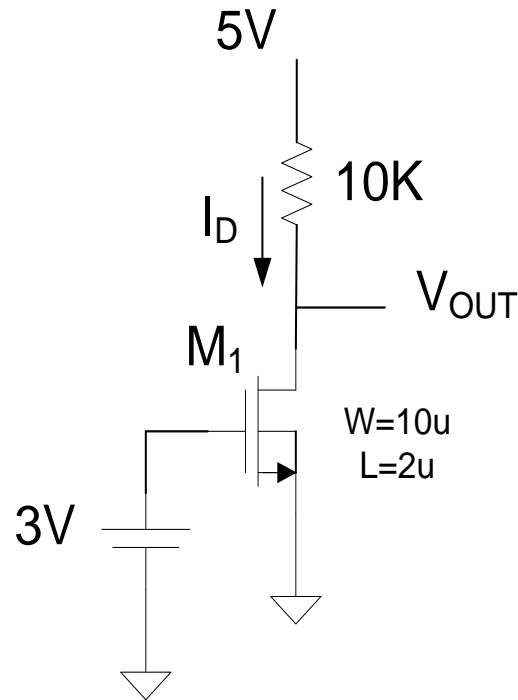
Solution:

Since $V_{GS} > V_T$, M_1 is operating in either saturation or triode region

Strategy will be to guess region of operation, solve, and then verify region

Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T=1V$ and $\mu C_{OX}=100\mu AV^{-2}$

5V

I_D

10K

V_{OUT}

M_1

W=10u
L=2u

3V
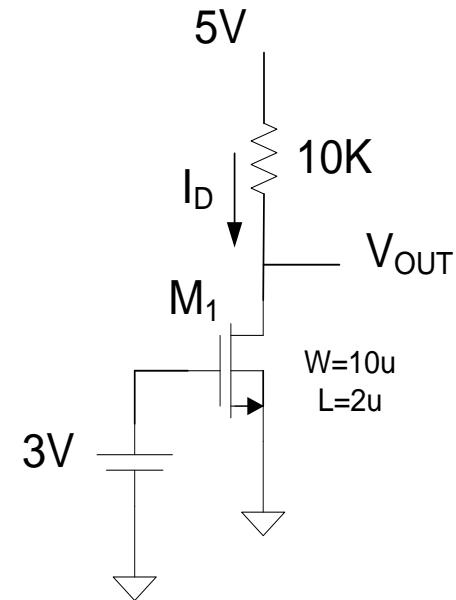
Solution:

Guess M_1 in saturation

$5V=I_D 10K+V_{OUT}$

$I_D = \dfrac{\mu C_{OX}W}{2L}(3-V_T)^2$

Required verification: $V_{DS}>V_{GS}-V_T$

Can eliminate I_D between these 2 equations to obtain V_{OUT}

Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T = 1V$ and $\mu C_{OX} = 100\mu AV^{-2}$

5V

I_D ⟩ 10K

V_{OUT}

M_1

W=10u
L=2u

3V

Guess M_1 in saturation

Required verification: $V_{DS} > V_{GS} - V_T$

$5V = I_D 10K + V_{OUT}$

$I_D = \dfrac{\mu C_{OX} W}{2L} (3 - V_T)^2$

$V_{OUT} = 5V - 10K \left[\dfrac{100\mu AV^{-2} 10\mu}{2 \bullet 2\mu} (2V)^2 \right]$

$V_{OUT} = -5V$

Verification: $V_{DS} = V_{OUT}$

-5 >? 2V - - 0 No! So verification fails and Guess of region is invalid

Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T = 1V$ and $\mu C_{OX} = 100\mu AV^{-2}$

Guess M_1 in triode
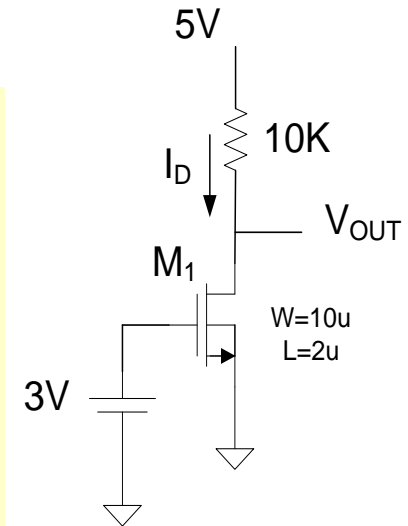
Required verification: $V_{DS} < V_{GS} - V_T$

$$5V = I_D 10K + V_{OUT}$$

$$I_D = \frac{\mu C_{OX} W}{L}\left(3 - V_T - \frac{V_{DS}}{2}\right)V_{DS}$$

$$V_{OUT} = 5V - 10K\left[\frac{100\mu AV^{-2} 10\mu}{2\mu}\left(2V - \frac{V_{OUT}}{2}\right)V_{OUT}\right]$$

$$V_{OUT} = 5V - \left[5\left(2V - \frac{V_{OUT}}{2}\right)V_{OUT}\right]$$

Solving for V_{OUT}, obtain

$$V_{OUT} = 0.515V$$

Verification: $V_{DS} = V_{OUT}$
0.515 <? 2V   Yes!   So verification succeeds and triode region is valid

$$V_{OUT} = 0.515V$$

5V

10K

I_D

V_{OUT}

M_1

W=10u
L=2u
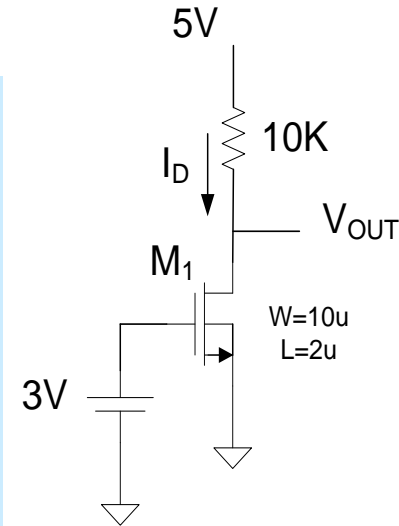
3V

Limitations of Existing Models
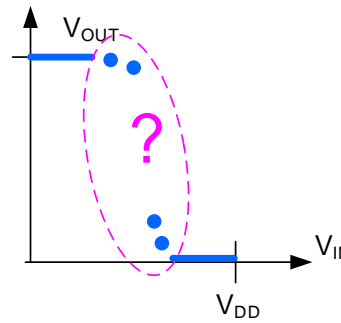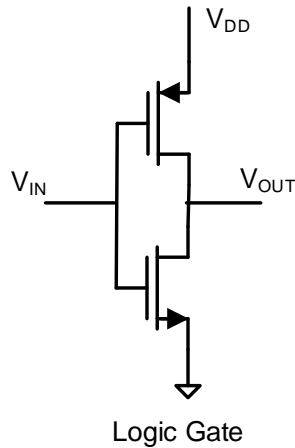
Logic Gate

Switch-Level Models

Simple square-law Model

Voltage Amplifier
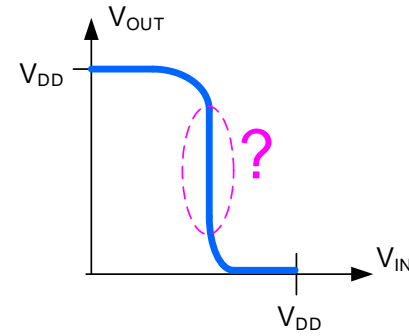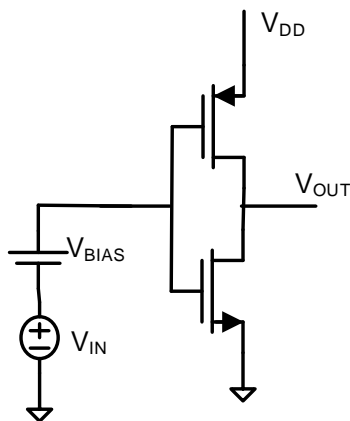
Switch-Level Models

Simple square-law Model

}

Voltage Gain
Input/Output Relationship ?

Model Extensions
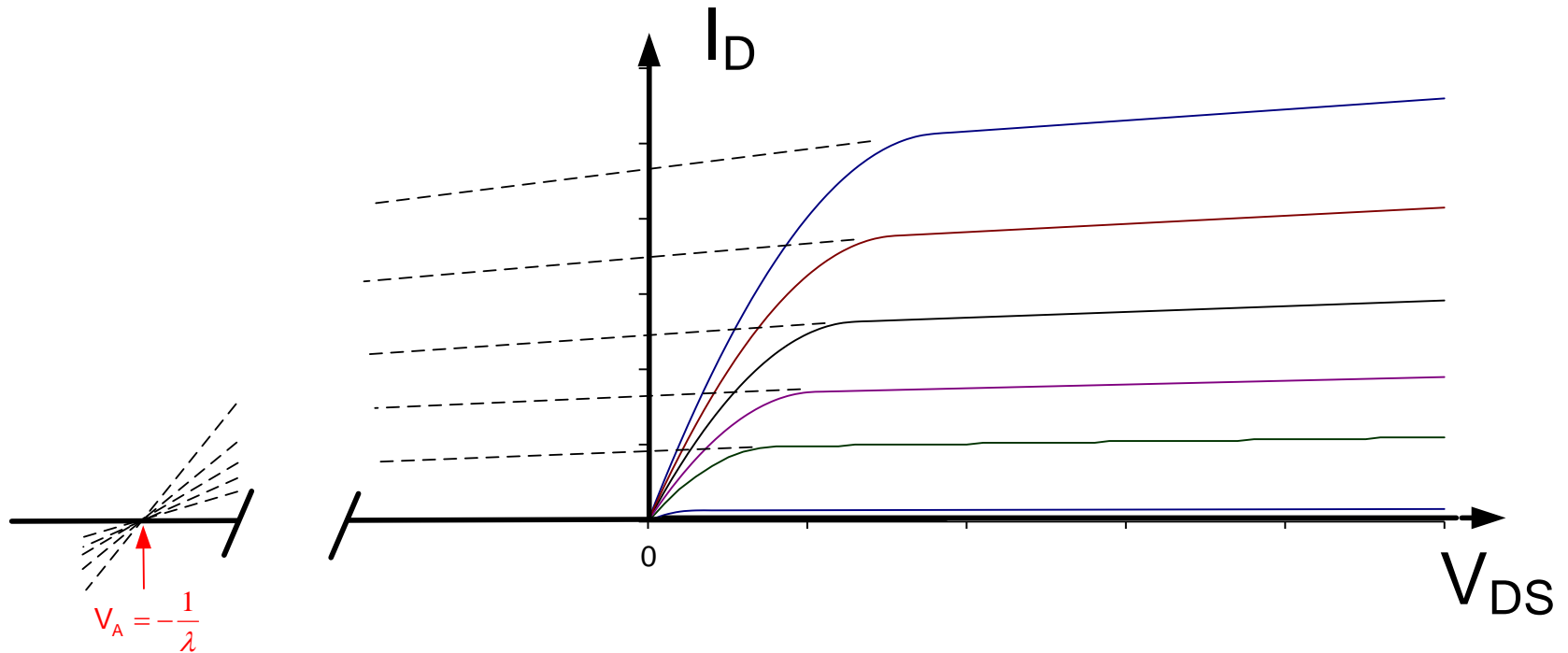
Projections intersect $-V_{DS}$ axis at same point, termed Early Voltage

Typical values from -20V to -200V

Usually use parameter λ instead of V_A in MOS model

Model Extensions
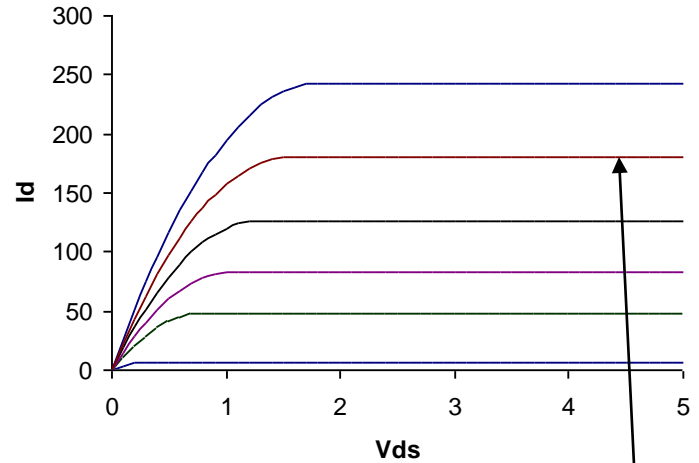
Existing Model

Slope is not 0
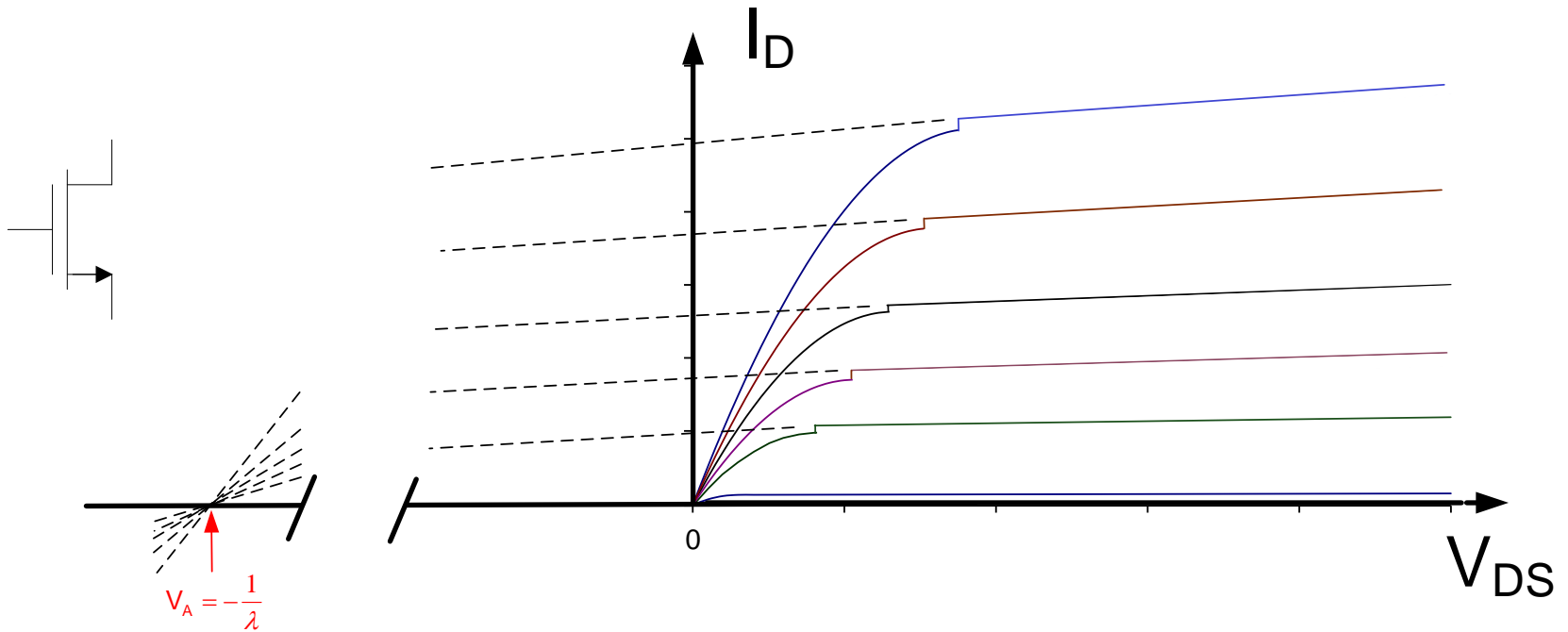
Actual Device

Model Extensions

$$I_D = \begin{cases} 0 & V_{GS} \le V_T \\ \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_T - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{OX} \dfrac{W}{2L}(V_{GS} - V_T)^2 \bullet (1 + \lambda V_{DS}) & V_{GS} \ge V_T \quad V_{DS} \ge V_{GS} - V_T \end{cases}$$

Note: This introduces small discontinuity in model at SAT/Triode transition

Further Model Extensions

Existing model does not depend upon the bulk voltage !

Observe that changing the bulk voltage will change the electric field in the channel region !
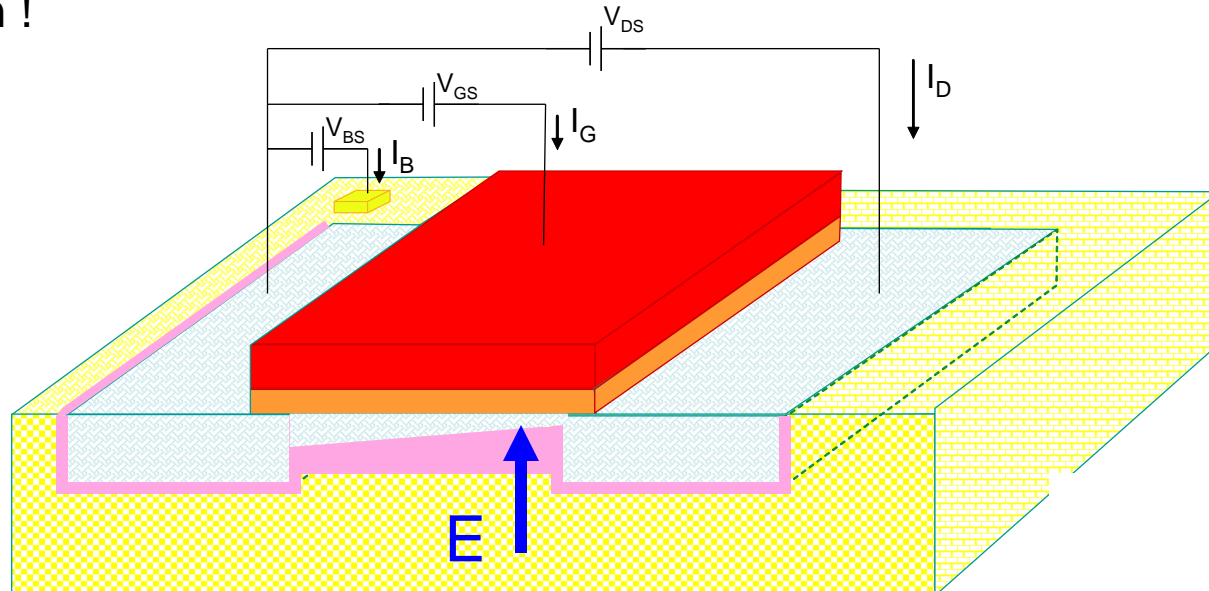
Further Model Extensions

Existing model does not depend upon the bulk voltage !

Observe that changing the bulk voltage will change the electric field in the channel region !
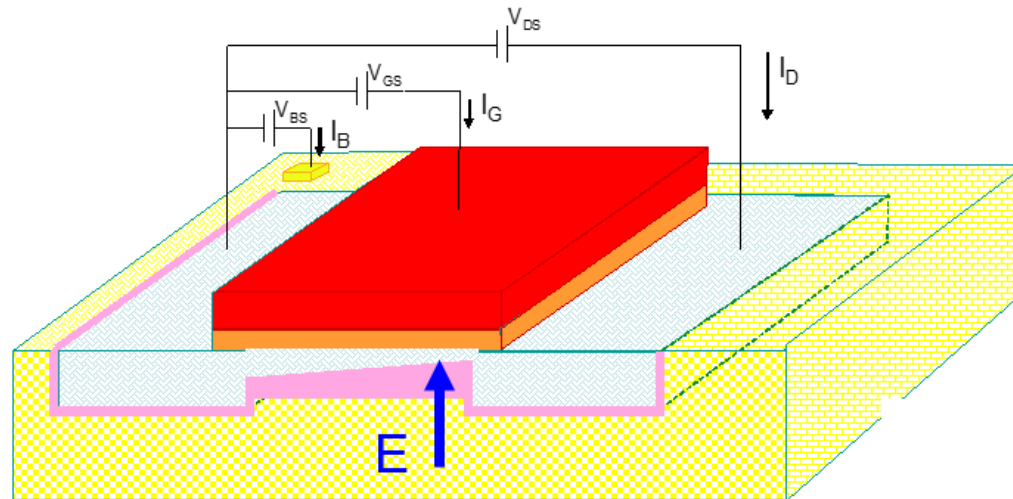
Changing the bulk voltage will change the thickness of the inversion layer

Changing the bulk voltage will change the threshold voltage of the device

$$V_T = V_{T0} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right)$$

Typical Bulk Effects on Threshold Voltage for n-channel Devices

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{\phi - V_{BS}} - \sqrt{\phi} \right)$$
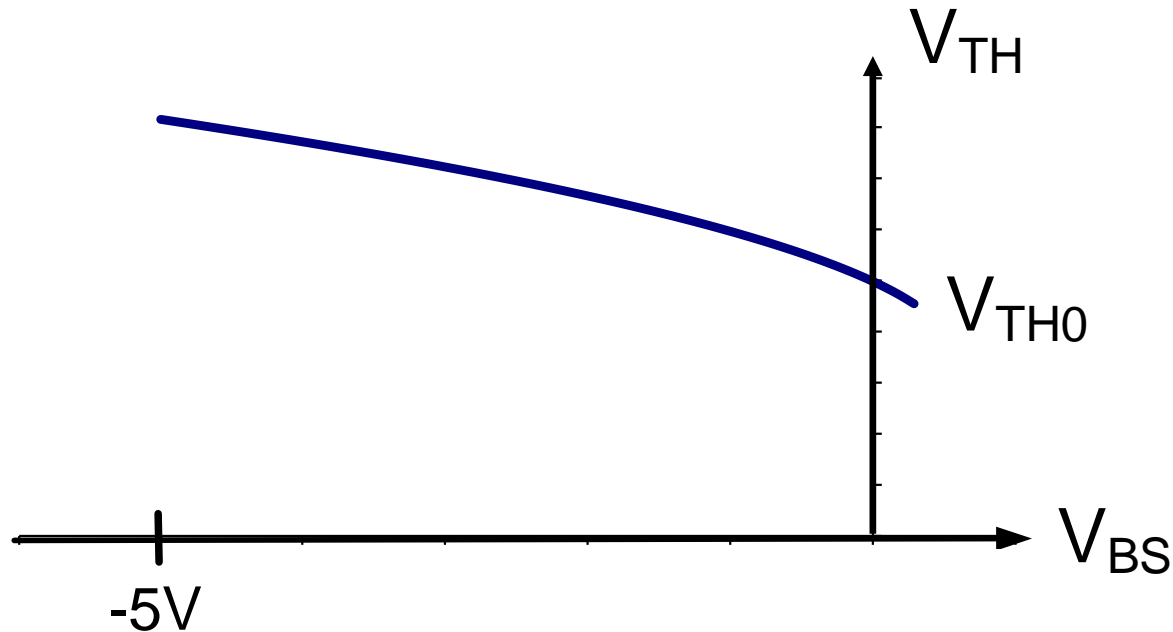
$$\gamma \cong 0.4 V^{1/2} \qquad \phi \cong 0.6V$$

- Bulk-Diffusion Generally Reverse Biased $(V_{BS}<0$ or at least $V_{BS}<0.3V$) for n-channel
- Shift in threshold voltage with bulk voltage can be substantial
- Often $V_{BS}=0$

Typical Bulk Effects on Threshold Voltage for n-channel Devices

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right)$$
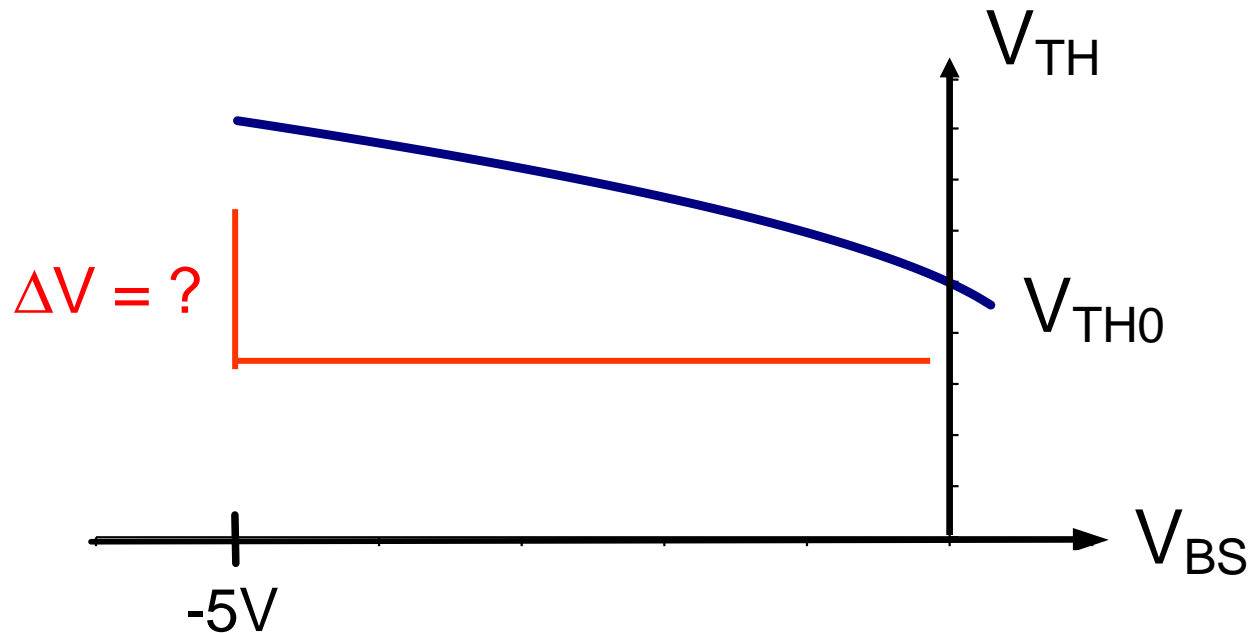
$$\gamma \cong 0.4V^{1/2} \qquad \phi \cong 0.6V$$

$$\Delta V = V_{TH} - V_{TH0} = \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right)$$

$$\Delta V \cong 0.4\left(\sqrt{0.6V - -5V} - \sqrt{0.6}\right) \cong 0.64V$$

Typical Bulk Effects on Threshold Voltage for p-channel Devices

$$V_{TH} = V_{TH0} - \gamma\left(\sqrt{\phi + V_{BS}} - \sqrt{\phi}\right)$$

$$\gamma \cong 0.4V^{1/2} \qquad \phi \cong 0.6V$$
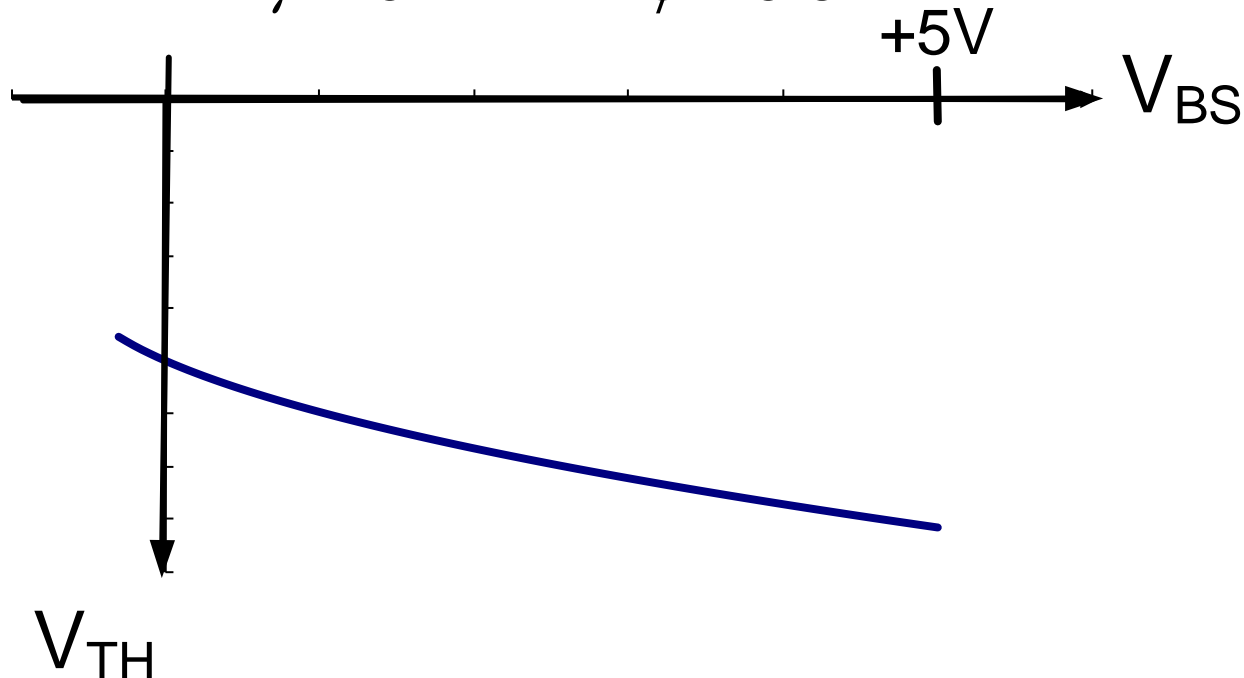
- Bulk-Diffusion Generally Reverse Biased $_{(V_{BS}>0 \text{ or at least } V_{BS}>-0.3V\,)}$ for p-channel
- Same functional form as for n-channel but $V_{TH0}<0$
- Magnitude of threshold voltage increases with magnitude of reverse bias

Model Extension Summary

$I_G = 0$

$I_B = 0$
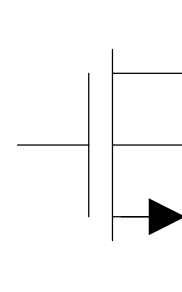
$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_T - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_T\right)^2 \bullet \left(1 + \lambda V_{DS}\right) & V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T \end{cases}$$

$$V_T = V_{T0} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right)$$

Model Parameters : $\{\mu, C_{OX}, V_{T0}, \varphi, \gamma, \lambda\}$

Design Parameters : $\{W, L\}$ but only one degree of freedom W/L
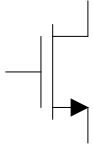
Operation Regions by Applications
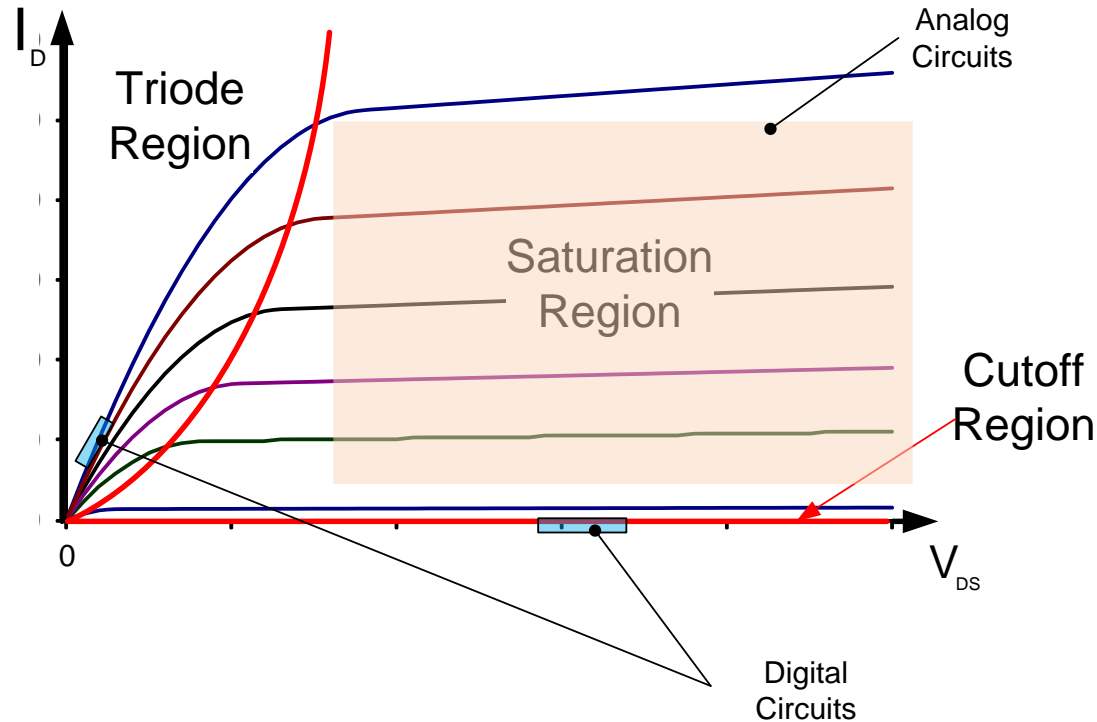
Most analog circuits operate in the saturation region

(basic VVR operates in triode and is an exception)

Most digital circuits operate in triode and cutoff regions and switch between these two with Boolean inputs

Model Extension (short devices)

$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_T - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_T\right)^2 & V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T \end{cases}$$

As the channel length becomes very short, velocity saturation will occur in the channel and this will occur with electric fields around 2V/u.   So, if a gate length is around 1u, then voltages up to 2V can be applied without velocity saturation.   But, if gate length decreases and voltages are kept high, velocity saturation will occur

$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \dfrac{\theta_2}{\theta_1} \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_T\right)^{\frac{\alpha}{2}} V_{DS} & V_{GS} \geq V_T \quad V_{DS} < \theta_1\left(V_{GS} - V_T\right)^{\frac{\alpha}{2}} \\ \theta_2 \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_T\right)^{\alpha} & V_{GS} \geq V_T \quad V_{DS} \geq \theta_1\left(V_{GS} - V_T\right)^{\frac{\alpha}{2}} \end{cases}$$

α is the velocity saturation index, 2 ≥ α ≥ 1

Model Extension (short devices)

(n-channel device)

$$
I_D = \begin{cases} 0 & V_{GS} \leq V_T \\[2ex] \dfrac{\theta_2}{\theta_1}\mu C_{OX}\dfrac{W}{L}\left(V_{GS}-V_T\right)^{\frac{\alpha}{2}}V_{DS} & V_{GS} \geq V_T \quad V_{DS} < \theta_1\left(V_{GS}-V_T\right)^{\frac{\alpha}{2}} \\[2ex] \theta_2\mu C_{OX}\dfrac{W}{L}\left(V_{GS}-V_T\right)^{\alpha} & V_{GS} \geq V_T \quad V_{DS} \geq \theta_1\left(V_{GS}-V_T\right)^{\frac{\alpha}{2}} \end{cases}
$$

α is the velocity saturation index, 2 ≥ α ≥ 1

No longer a square-law model (some term it an α-power model)

For long devices, α=2

Channel length modulation (λ) and bulk effects can be added to the velocity Saturation as well

Degrading of α is not an attractive limitation of the MOSFET

Model Extension (BSIM model)

```
.MODEL CMOSN NMOS (                                          LEVEL     = 49
+VERSION = 3.1            TNOM      = 27                      TOX       = 1.42E-8
+XJ      = 1.5E-7         NCH       = 1.7E17                  VTHO      = 0.629035
+K1      = 0.8976376      K2        = -0.09255                K3        = 24.0984767
+K3B     = -8.2369696     W0        = 1.041146E-8             NLX       = 1E-9
+DVTOW   = 0              DVT1W     = 0                        DVT2W     = 0
+DVT0    = 2.7123969      DVT1      = 0.4232931               DVT2      = -0.1403765
+U0      = 451.2322004    UA        = 3.091785E-13            UB        = 1.702517E-18
+UC      = 1.22401E-11    VSAT      = 1.715884E5              A0        = 0.6580918
+AGS     = 0.130484       B0        = 2.446405E-6             B1        = 5E-6
+KETA    = -3.043349E-3   A1        = 8.18159E-7              A2        = 0.3363058
+RDSW    = 1.367055E3     PRWG      = 0.0328586               PRWB      = 0.0104806
+WR      = 1              WINT      = 2.443677E-7             LINT      = 6.999776E-8
+XL      = 1E-7           XW        = 0                       DWG       = -1.256454E-8
+DWB     = 3.676235E-8    VOFF      = -1.493503E-4            NFACTOR = 1.0354201
+CIT     = 0              CDSC      = 2.4E-4                   CDSCD     = 0
+CDSCB   = 0              ETA0      = 2.342963E-3             ETAB      = -1.5324E-4
+DSUB    = 0.0764123      PCLM      = 2.5941582               PDIBLC1 = 0.8187825
+PDIBLC2 = 2.366707E-3    PDIBLCB   = -0.0431505             DROUT     = 0.9919348
+PSCBE1  = 6.611774E8     PSCBE2    = 3.238266E-4             PVAG      = 0

+PRT     = 0              UTE       = -1.5                    KT1       = -0.11
+KT1L    = 0              KT2       = 0.022                   UA1       = 4.31E-9
+UB1     = -7.61E-18      UC1       = -5.6E-11                AT        = 3.3E4
+WL      = 0              WLN       = 1                       WW        = 0
+WWN     = 1              WWL       = 0                       LL        = 0
+LLN     = 1              LW        = 0                        LWN       = 1
+LWL     = 0              CAPMOD    = 2                       XPART     = 0.5
+CGDO    = 2.32E-10       CGSO      = 2.32E-10                CGBO      = 1E-9
+CJ      = 4.282017E-4    PB        = 0.9317787               MJ        = 0.4495867
+CJSW    = 3.034055E-10   PBSW      = 0.8                     MJSW      = 0.1713852
+CJSWG   = 1.64E-10       PBSWG     = 0.8                     MJSWG     = 0.1713852
+CF      = 0              PVTHO     = 0.0520855               PRDSW     = 112.8875816
+PK2     = -0.0289036     WKETA     = -0.0237483              LKETA     = 1.728324E-3      )
*
```
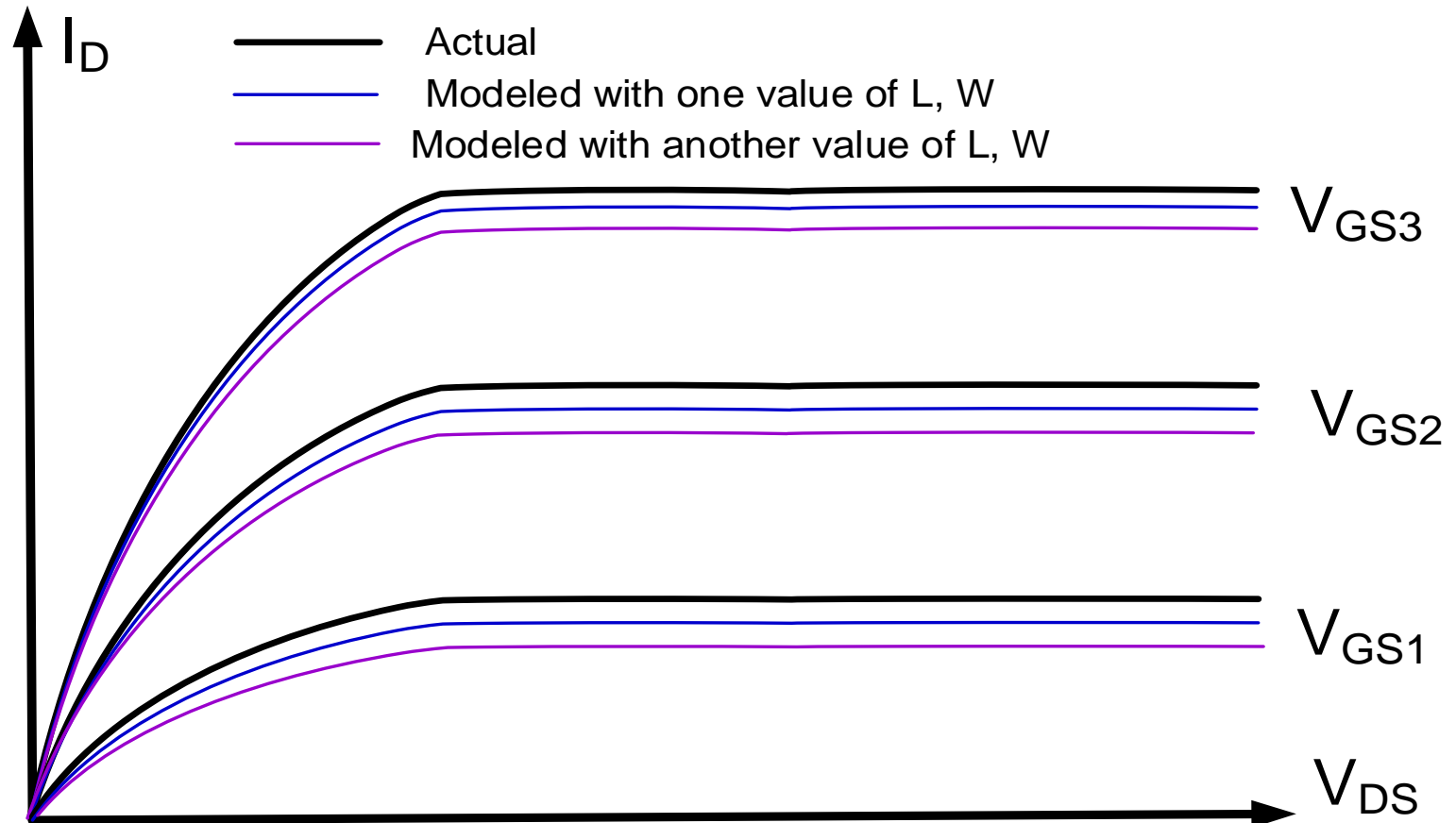
Model Errors with Different W/L Values

Binning models can improve model accuracy

BSIM Binning Model

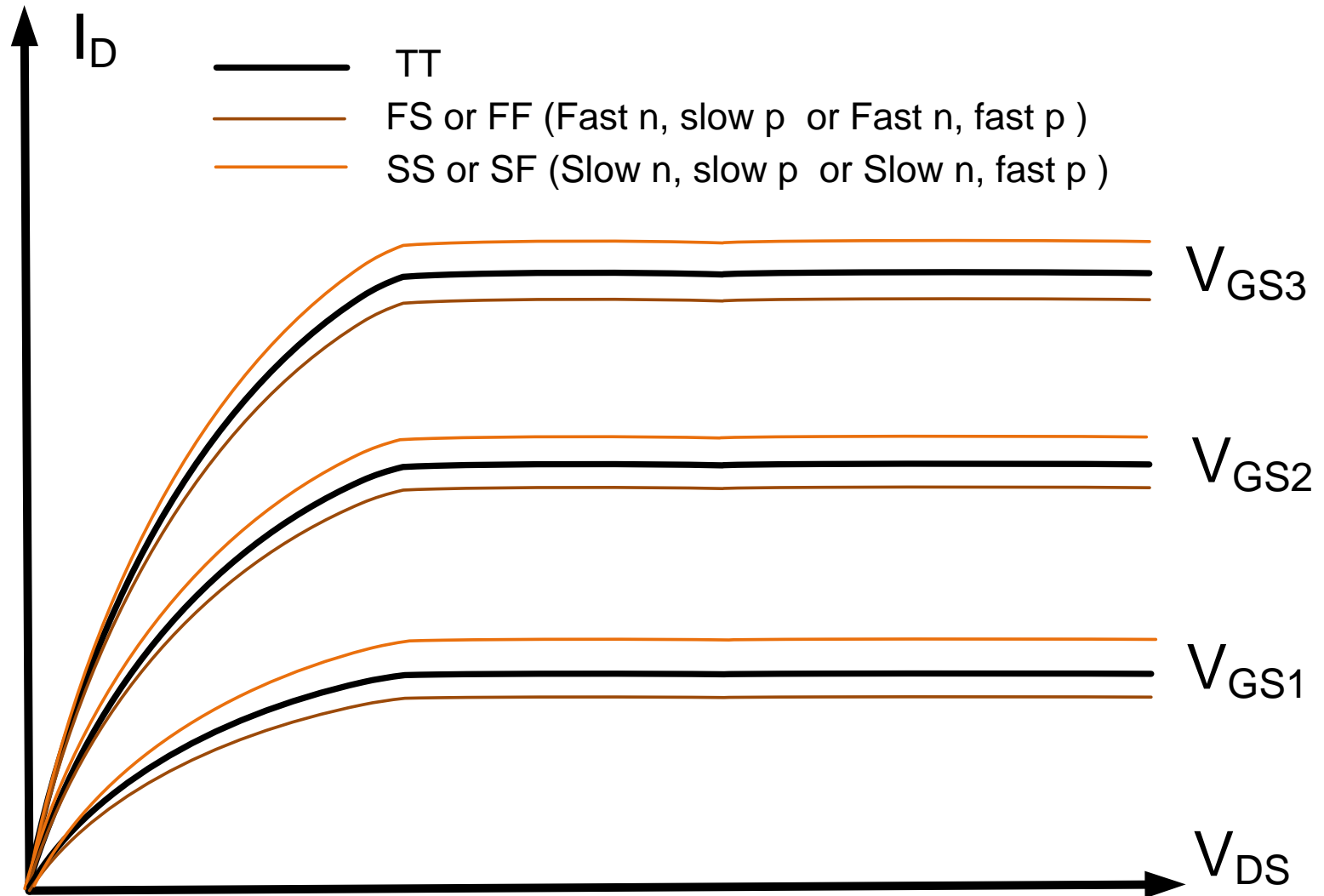- Bin on device sizes

- multiple BSIM models !

```
.MODEL CMOSN NMOS (                                        LEVEL    = 49
+VERSION = 3.1           TNOM      = 27            TOX      = 1.42E-8
+XJ      = 1.5E-7        NCH       = 1.7E17        VTH0     = 0.629035
+K1      = 0.8976376     K2        = -0.09255      K3       = 24.0984767
+K3B     = -8.2369696    W0        = 1.041146E-8   NLX      = 1E-9
+DVT0W   = 0             DVT1W     = 0             DVT2W    = 0
+DVT0    = 2.7123969     DVT1      = 0.4232931     DVT2     = -0.1403765
+U0      = 451.2322004   UA        = 3.091785E-13  UB       = 1.702517E-18
+UC      = 1.22401E-11   VSAT      = 1.715884E5    A0       = 0.6580918
+AGS     = 0.130484      B0        = 2.446405E-6   B1       = 5E-6
+KETA    = -3.043349E-3  A1        = 8.18159E-7    A2       = 0.3363058
+RDSW    = 1.367055E3    PRWG      = 0.0328586     PRWB     = 0.0104806
+WR      = 1             WINT      = 2.443677E-7   LINT     = 6.999776E-8
+XL      = 1E-7          XW        = 0             DWG      = -1.256454E-8
+DWB     = 3.676235E-8   VOFF      = -1.493503E-4  NFACTOR  = 1.0354201
+CIT     = 0             CDSC      = 2.4E-4        CDSCD    = 0
+CDSCB   = 0             ETA0      = 2.342963E-3   ETAB     = -1.5324E-4
+DSUB    = 0.0764123     PCLM      = 2.5941582     PDIBLC1  = 0.8187825
+PDIBLC2 = 2.366707E-3   PDIBLCB   = -0.0431505    DROUT    = 0.9919348
+PSCBE1  = 6.611774E8    PSCBE2    = 3.238266E-4   PVAG     = 0

+PRT     = 0             UTE       = -1.5          KT1      = -0.11
+KT1L    = 0             KT2       = 0.022         UA1      = 4.31E-9
+UB1     = -7.61E-18     UC1       = -5.6E-11      AT       = 3.3E4
+WL      = 0             WLN       = 1             WW       = 0
+WWN     = 1             WWL       = 0             LL       = 0
+LLN     = 1             LW        = 0             LWN      = 1
+LWL     = 0             CAPMOD    = 2             XPART    = 0.5
+CGDO    = 2.32E-10      CGSO      = 2.32E-10      CGBO     = 1E-9
+CJ      = 4.282017E-4   PB        = 0.9317787     MJ       = 0.4495867
+CJSW    = 3.034055E-10  PBSW      = 0.8           MJSW     = 0.1713852
+CJSWG   = 1.64E-10      PBSWG     = 0.8           MJSWG    = 0.1713852
+CF      = 0             PVTH0     = 0.0520855     PRDSW    = 112.8875816
+PK2     = -0.0289036    WKETA     = -0.0237483    LKETA    = 1.728324E-3  )
*
```

With 32 bins, this model has 3040 model parameters !

Model Changes with Process Variations

(n-ch characteristics shown)

Corner models can improve model accuracy

BSIM Corner Models with Binning

- Often 4 corners in addition to nominal TT, FF, FS, SF, and SS

- bin on device sizes

```
.MODEL CMOSN NMOS (                                       LEVEL    = 49
+VERSION = 3.1           TNOM      = 27          TOX      = 1.42E-8
+XJ      = 1.5E-7        NCH       = 1.7E17      VTH0     = 0.629035
+K1      = 0.8976376     K2        = -0.09255    K3       = 24.0984767
+K3B     = -8.2369696    W0        = 1.041146E-8 NLX      = 1E-9
+DVT0W   = 0             DVT1W     = 0           DVT2W    = 0
+DVT0    = 2.7123969     DVT1      = 0.4232931   DVT2     = -0.1403765
+U0      = 451.2322004   UA        = 3.091785E-13 UB      = 1.702517E-18
+UC      = 1.22401E-11   VSAT      = 1.715884E5  A0       = 0.6580918
+AGS     = 0.130484      B0        = 2.446405E-6 B1       = 5E-6
+KETA    = -3.043349E-3  A1        = 8.18159E-7  A2       = 0.3363058
+RDSW    = 1.367055E3    PRWG      = 0.0328586   PRWB     = 0.0104806
+WR      = 1             WINT      = 2.443677E-7 LINT     = 6.999776E-8
+XL      = 1E-7          XW        = 0           DWG      = -1.256454E-8
+DWB     = 3.676235E-8   VOFF      = -1.493503E-4 NFACTOR = 1.0354201
+CIT     = 0             CDSC      = 2.4E-4      CDSCD    = 0
+CDSCB   = 0             ETA0      = 2.342963E-3 ETAB     = -1.5324E-4
+DSUB    = 0.0764123     PCLM      = 2.5941582  PDIBLC1  = 0.8187825
+PDIBLC2 = 2.366707E-3   PDIBLCB   = -0.0431505 DROUT    = 0.9919348
+PSCBE1  = 6.611774E8    PSCBE2    = 3.238266E-4 PVAG     = 0
+DELTA   = 0.01          RSH       = 83.5        MOBMOD   = 1
 +PRT     = 0             UTE       = -1.5        KT1      = -0.11
 +KT1L    = 0             KT2       = 0.022       UA1      = 4.31E-9
 +UB1     = -7.61E-18     UC1       = -5.6E-11    AT       = 3.3E4
 +WL      = 0             WLN       = 1           WW       = 0
 +WWN     = 1             WWL       = 0           LL       = 0
 +LLN     = 1             LW        = 0           LWN      = 1
 +LWL     = 0             CAPMOD    = 2           XPART    = 0.5
 +CGDO    = 2.32E-10      CGSO      = 2.32E-10    CGBO     = 1E-9
 +CJ      = 4.282017E-4   PB        = 0.9317787   MJ       = 0.4495867
 +CJSW    = 3.034055E-10  PBSW      = 0.8         MJSW     = 0.1713852
 +CJSWG   = 1.64E-10      PBSWG     = 0.8         MJSWG    = 0.1713852
 +CF      = 0             PVTH0     = 0.0520855   PRDSW    = 112.8875816
 +PK2     = -0.0289036    WKETA     = -0.0237483  LKETA    = 1.728324E-3      )
 *
```

With 32 size bins and 4 corners, this model has 15,200 model parameters !

How many models of the MOSFET do we have?

Switch-level model (2)

Square-law model

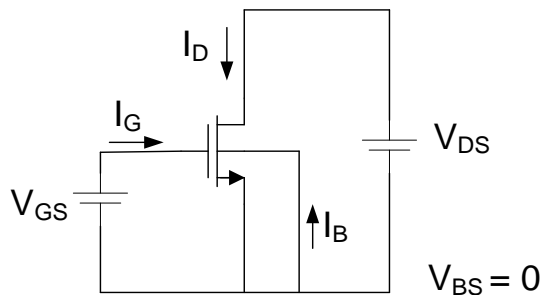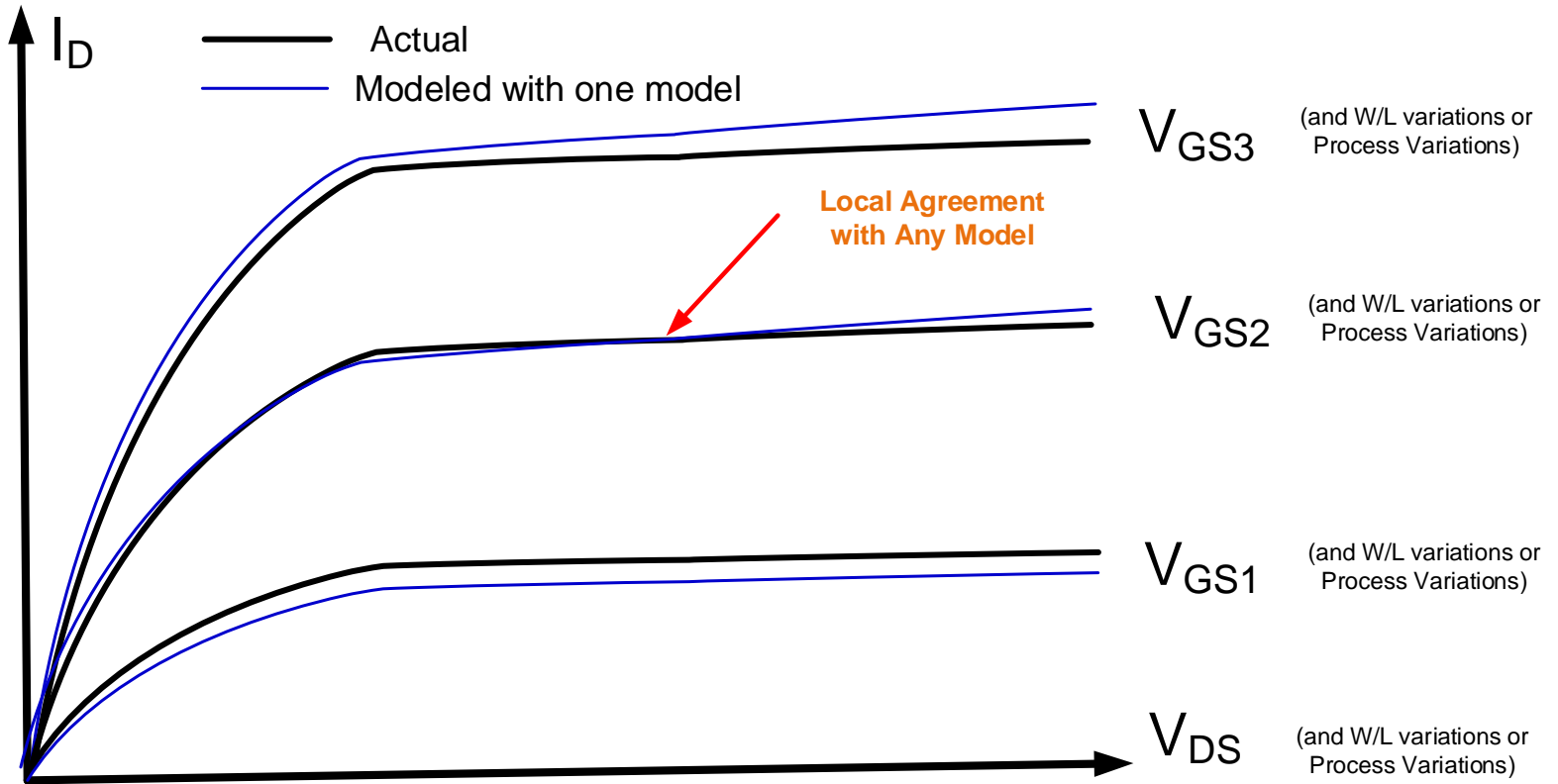Square-law model (with λ and bulk additions)

α-law model (with λ and bulk additions)

BSIM model

BSIM model (with binning extensions)

BSIM model (with binning extensions and process corners)

The Modeling Challenge

Legend:
- **Actual** (thick black line)
- Modeled with one model (thin blue line)

V_{GS3} (and W/L variations or Process Variations)

Local Agreement with Any Model

V_{GS2} (and W/L variations or Process Variations)

V_{GS1} (and W/L variations or Process Variations)

V_{DS} (and W/L variations or Process Variations)

Circuit with I_D, I_G, V_{GS}, V_{DS}, I_B, $V_{BS} = 0$

$$I_D = f_1\left(V_{GS}, V_{DS}\right)$$
$$I_G = f_2\left(V_{GS}, V_{DS}\right)$$
$$I_B = f_3\left(V_{GS}, V_{DS}\right)$$

Difficult to obtain analytical functions that accurately fit actual devices over bias, size, and process variations
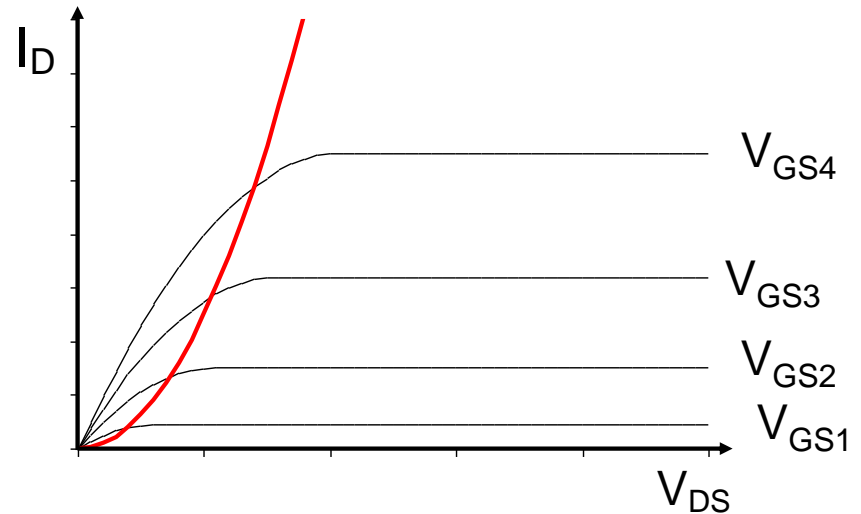
Model Status
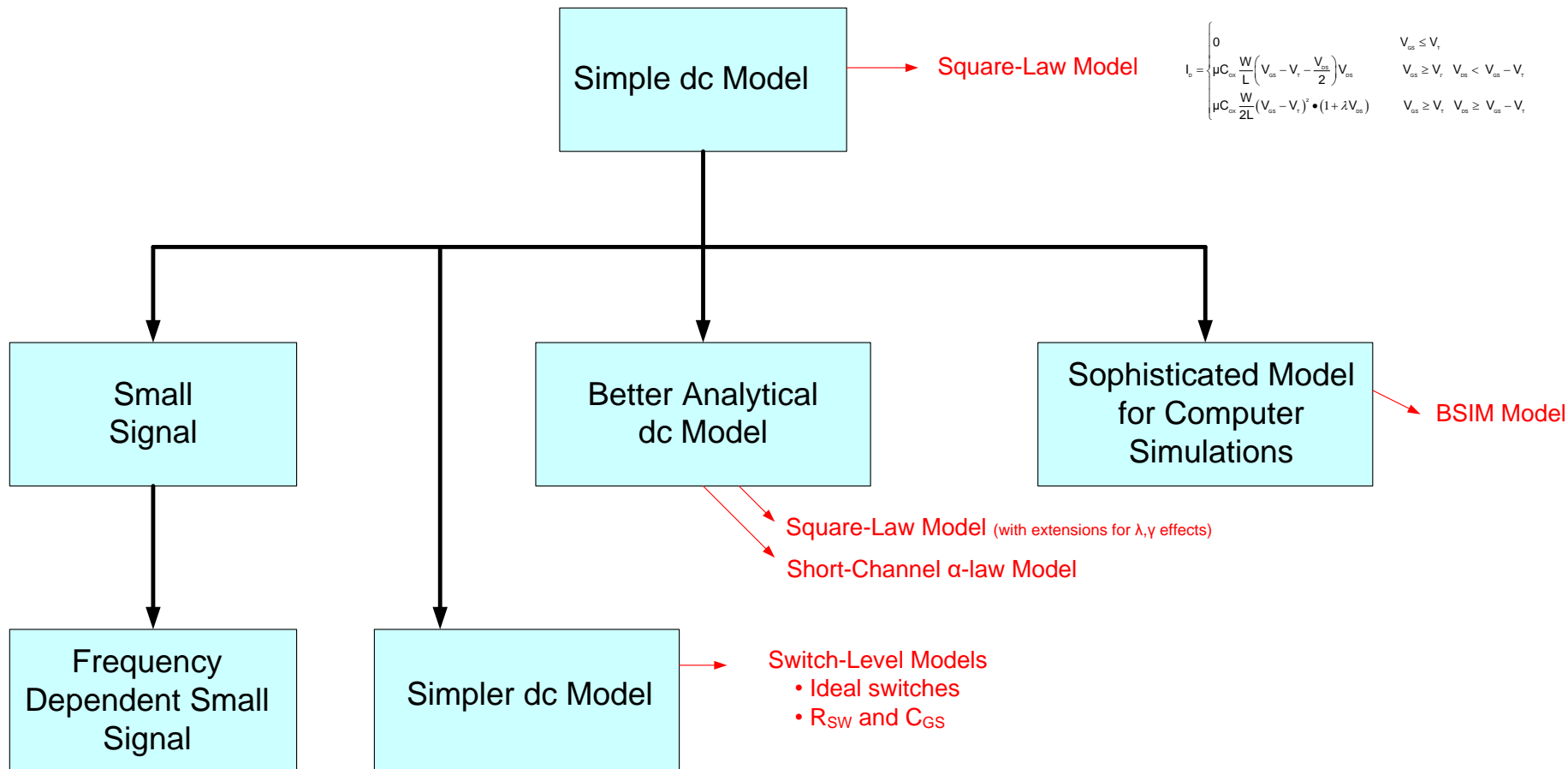
In the next few slides, the models we have developed will be listed and reviewed

- Square-law Model
- Switch-level Models
- Extended Square-law model
- Short-channel model
- BSIM Model
- BSIM Binning Model
- Corner Models

Square-Law Model

$$I_D = \begin{cases} 0 & V_{GS} \le V_T \\ \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_T - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_T\right)^2 & V_{GS} \ge V_T \quad V_{DS} \ge V_{GS} - V_T \end{cases}$$

Model Parameters : $\{\mu, C_{OX}, V_{T0}\}$

Design Parameters : $\{W, L\}$ but only one degree of freedom W/L

Switch-Level Models

Switch-level model including gate capacitance and drain resistance

C_{GS} and R_{SW} dependent upon device sizes and process

For minimum-sized devices in a 0.5u process

$$\mathbf{C_{GS} \cong 1.5fF} \qquad \mathbf{R_{sw} \cong} \quad \begin{cases} \mathbf{2K\Omega \ \ n-channel} \\ \mathbf{6K\Omega \ \ p-channel} \end{cases}$$

Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

Model Parameters : $\{C_{GS}, R_{SW}\}$
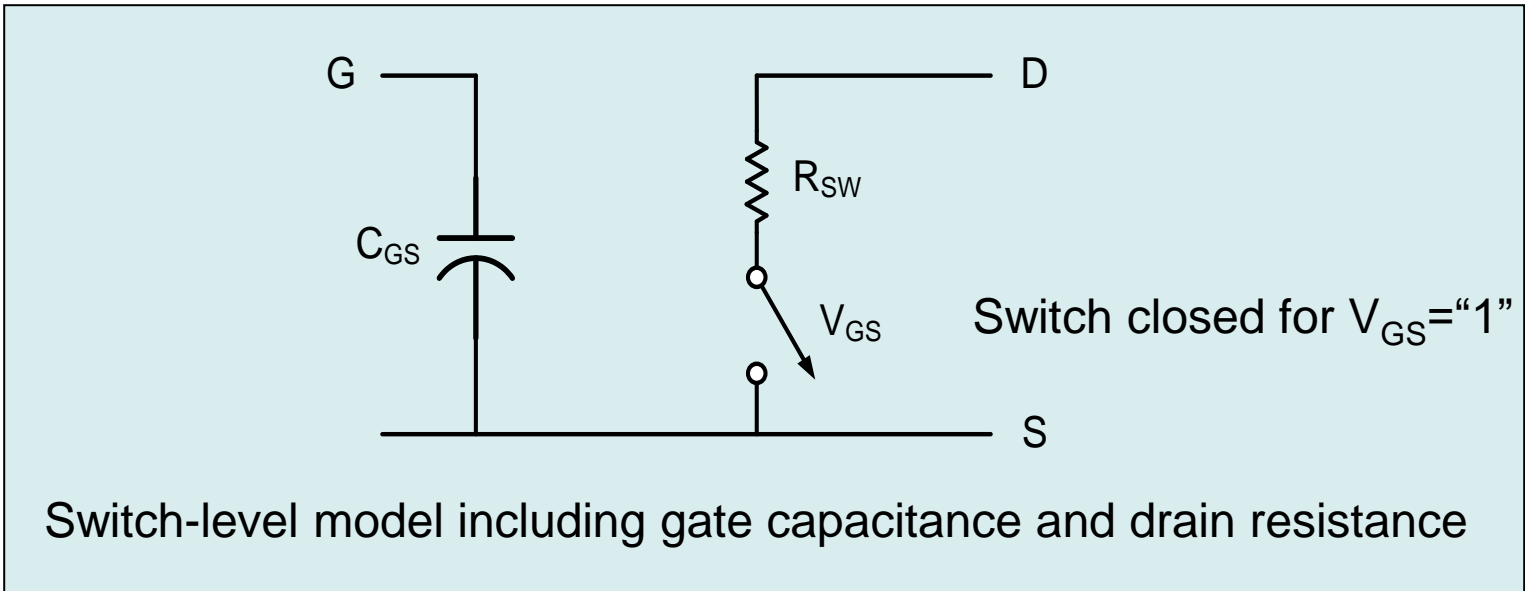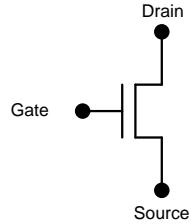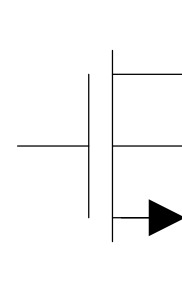
Extended Square-Law Model

$I_G = 0$

$I_B = 0$

$$I_D = \begin{cases} 0 & V_{GS} \le V_T \\ \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_T - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_T\right)^2 \bullet \left(1 + \lambda V_{DS}\right) & V_{GS} \ge V_T \quad V_{DS} \ge V_{GS} - V_T \end{cases}$$

$$V_T = V_{T0} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right)$$

Model Parameters : $\{\mu, C_{OX}, V_{T0}, \varphi, \gamma, \lambda\}$

Design Parameters : $\{W,L\}$ but only one degree of freedom W/L

Short-Channel Model

$$I_D = \begin{cases} 0 & V_{GS} \le V_T \\ \dfrac{\theta_2}{\theta_1} \mu C_{OX} \dfrac{W}{L} \left(V_{GS} - V_T\right)^{\frac{\alpha}{2}} V_{DS} & V_{GS} \ge V_T \quad V_{DS} < \theta_1 \left(V_{GS} - V_T\right)^{\frac{\alpha}{2}} \\ \theta_2 \mu C_{OX} \dfrac{W}{L} \left(V_{GS} - V_T\right)^{\alpha} & V_{GS} \ge V_T \quad V_{DS} \ge \theta_1 \left(V_{GS} - V_T\right)^{\frac{\alpha}{2}} \end{cases}$$

α is the velocity saturation index, 2 ≥ α ≥ 1

Channel length modulation (λ) and bulk effects can be added to the velocity
Saturation as well

BSIM model

```
.MODEL CMOSN NMOS (                                        LEVEL    = 49
+VERSION = 3.1          TNOM     = 27          TOX      = 1.42E-8
+XJ      = 1.5E-7       NCH      = 1.7E17      VTH0     = 0.629035
+K1      = 0.8976376    K2       = -0.09255    K3       = 24.0984767
+K3B     = -8.2369696   W0       = 1.041146E-8 NLX      = 1E-9
+DVT0W   = 0            DVT1W    = 0           DVT2W    = 0
+DVT0    = 2.7123969    DVT1     = 0.4232931   DVT2     = -0.1403765
+U0      = 451.2322004  UA       = 3.091785E-13 UB      = 1.702517E-18
+UC      = 1.22401E-11  VSAT     = 1.715884E5  A0       = 0.6580918
+AGS     = 0.130484     B0       = 2.446405E-6 B1       = 5E-6
+KETA    = -3.043349E-3 A1       = 8.18159E-7  A2       = 0.3363058
+RDSW    = 1.367055E3   PRWG     = 0.0328586   PRWB     = 0.0104806
+WR      = 1            WINT     = 2.443677E-7 LINT     = 6.999776E-8
+XL      = 1E-7         XW       = 0           DWG      = -1.256454E-8
+DWB     = 3.676235E-8  VOFF     = -1.493503E-4 NFACTOR = 1.0354201
+CIT     = 0            CDSC     = 2.4E-4      CDSCD    = 0
+CDSCB   = 0            ETA0     = 2.342963E-3 ETAB     = -1.5324E-4
+DSUB    = 0.0764123    PCLM     = 2.5941582  PDIBLC1  = 0.8187825
+PDIBLC2 = 2.366707E-3  PDIBLCB  = -0.0431505 DROUT    = 0.9919348
+PSCBE1  = 6.611774E8   PSCBE2   = 3.238266E-4 PVAG     = 0

+PRT     = 0            UTE      = -1.5        KT1      = -0.11
+KT1L    = 0            KT2      = 0.022       UA1      = 4.31E-9
+UB1     = -7.61E-18    UC1      = -5.6E-11    AT       = 3.3E4
+WL      = 0            WLN      = 1           WW       = 0
+WWN     = 1            WWL      = 0           LL       = 0
+LLN     = 1            LW       = 0           LWN      = 1
+LWL     = 0            CAPMOD   = 2           XPART    = 0.5
+CGDO    = 2.32E-10     CGSO     = 2.32E-10    CGBO     = 1E-9
+CJ      = 4.282017E-4  PB       = 0.9317787  MJ       = 0.4495867
+CJSW    = 3.034055E-10 PBSW     = 0.8         MJSW     = 0.1713852
+CJSWG   = 1.64E-10     PBSWG    = 0.8         MJSWG    = 0.1713852
+CF      = 0            PVTH0    = 0.0520855   PRDSW    = 112.8875816
+PK2     = -0.0289036   WKETA    = -0.0237483  LKETA    = 1.728324E-3  )
*
```

Note this model has 95 model parameters !

BSIM Binning Model

- Bin on device sizes

- multiple BSIM models !

```
.MODEL CMOSN NMOS (                                              LEVEL    = 49
+VERSION = 3.1          TNOM     = 27             TOX      = 1.42E-8
+XJ      = 1.5E-7       NCH      = 1.7E17         VTH0     = 0.629035
+K1      = 0.8976376    K2       = -0.09255       K3       = 24.0984767
+K3B     = -8.2369696   W0       = 1.041146E-8    NLX      = 1E-9
+DVT0W   = 0            DVT1W    = 0              DVT2W    = 0
+DVT0    = 2.7123969    DVT1     = 0.4232931      DVT2     = -0.1403765
+U0      = 451.2322004  UA       = 3.091785E-13   UB       = 1.702517E-18
+UC      = 1.22401E-11  VSAT     = 1.715884E5     A0       = 0.6580918
+AGS     = 0.130484     B0       = 2.446405E-6    B1       = 5E-6
+KETA    = -3.043349E-3 A1       = 8.18159E-7     A2       = 0.3363058
+RDSW    = 1.367055E3   PRWG     = 0.0328586      PRWB     = 0.0104806
+WR      = 1            WINT     = 2.443677E-7    LINT     = 6.999776E-8
+XL      = 1E-7         XW       = 0              DWG      = -1.256454E-8
+DWB     = 3.676235E-8  VOFF     = -1.493503E-4   NFACTOR  = 1.0354201
+CIT     = 0            CDSC     = 2.4E-4         CDSCD    = 0
+CDSCB   = 0            ETA0     = 2.342963E-3    ETAB     = -1.5324E-4
+DSUB    = 0.0764123    PCLM     = 2.5941582      PDIBLC1  = 0.8187825
+PDIBLC2 = 2.366707E-3  PDIBLCB  = -0.0431505     DROUT    = 0.9919348
+PSCBE1  = 6.611774E8   PSCBE2   = 3.238266E-4    PVAG     = 0

+PRT     = 0            UTE      = -1.5           KT1      = -0.11
+KT1L    = 0            KT2      = 0.022          UA1      = 4.31E-9
+UB1     = -7.61E-18    UC1      = -5.6E-11       AT       = 3.3E4
+WL      = 0            WLN      = 1              WW       = 0
+WWN     = 1            WWL      = 0              LL       = 0
+LLN     = 1            LW       = 0              LWN      = 1
+LWL     = 0            CAPMOD   = 2              XPART    = 0.5
+CGDO    = 2.32E-10     CGSO     = 2.32E-10       CGBO     = 1E-9
+CJ      = 4.282017E-4  PB       = 0.9317787      MJ       = 0.4495867
+CJSW    = 3.034055E-10 PBSW     = 0.8            MJSW     = 0.1713852
+CJSWG   = 1.64E-10     PBSWG    = 0.8            MJSWG    = 0.1713852
+CF      = 0            PVTH0    = 0.0520855      PRDSW    = 112.8875816
+PK2     = -0.0289036   WKETA    = -0.0237483     LKETA    = 1.728324E-3    )
*
```

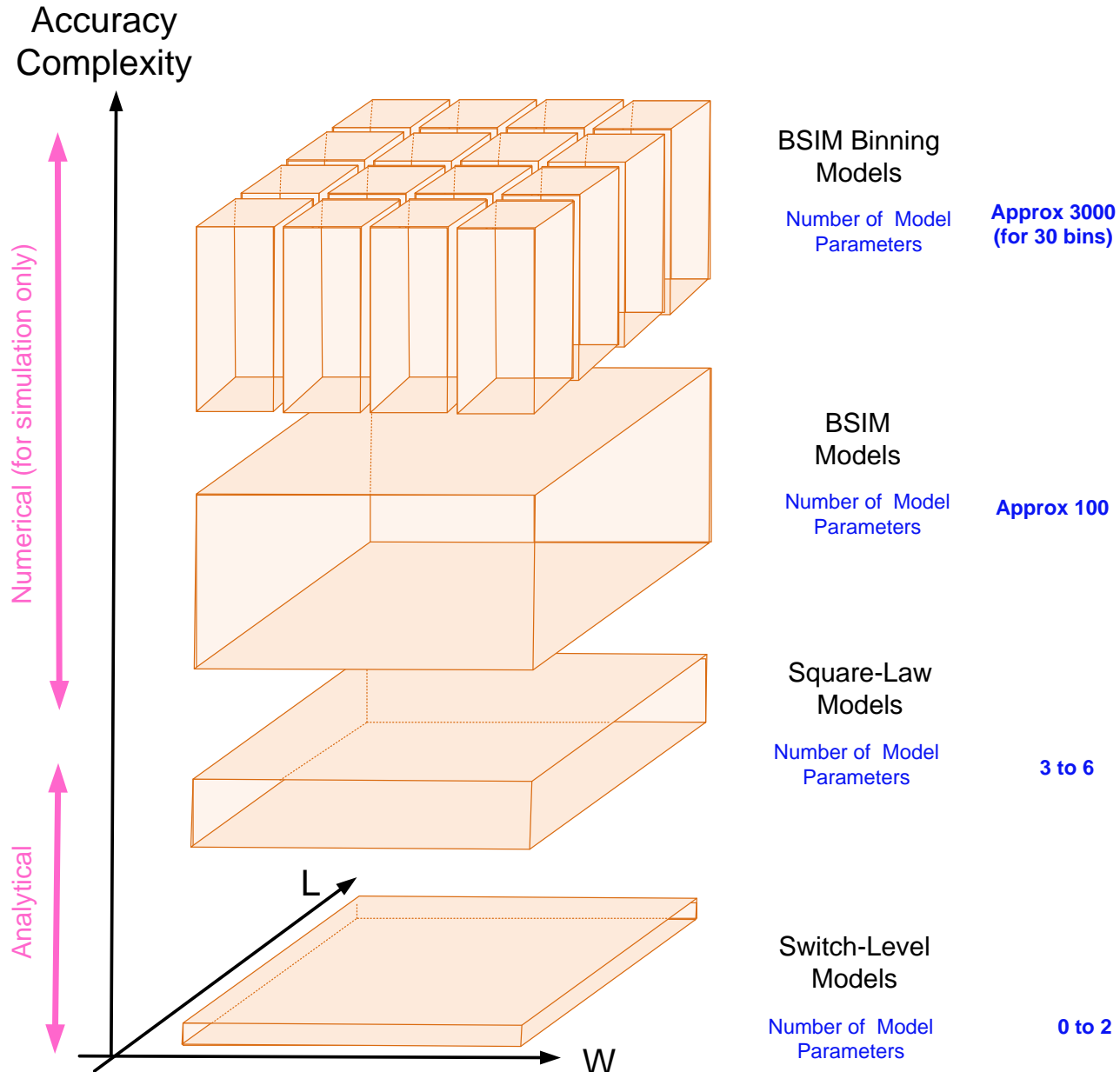With 32 bins, this model has 3040 model parameters !

BSIM Corner Models

- Often 4 corners in addition to nominal TT, FF, FS, SF, and SS

- five different BSIM models !

```
.MODEL CMOSN NMOS (                                    LEVEL      = 49
+VERSION = 3.1          TNOM      = 27              TOX        = 1.42E-8
+XJ       = 1.5E-7      NCH       = 1.7E17          VTH0       = 0.629035
+K1       = 0.8976376   K2        = -0.09255        K3         = 24.0984767
+K3B      = -8.2369696  W0        = 1.041146E-8     NLX        = 1E-9
+DVT0W    = 0           DVT1W     = 0               DVT2W      = 0
+DVT0     = 2.7123969   DVT1      = 0.4232931       DVT2       = -0.1403765
+U0       = 451.2322004 UA        = 3.091785E-13    UB         = 1.702517E-18
+UC       = 1.22401E-11 VSAT      = 1.715884E5      A0         = 0.6580918
+AGS      = 0.130484    B0        = 2.446405E-6     B1         = 5E-6
+KETA     = -3.043349E-3 A1       = 8.18159E-7      A2         = 0.3363058
+RDSW     = 1.367055E3  PRWG      = 0.0328586       PRWB       = 0.0104806
+WR       = 1           WINT      = 2.443677E-7     LINT       = 6.999776E-8
+XL       = 1E-7        XW        = 0               DWG        = -1.256454E-8
+DWB      = 3.676235E-8 VOFF      = -1.493503E-4    NFACTOR    = 1.0354201
+CIT      = 0           CDSC      = 2.4E-4          CDSCD      = 0
+CDSCB    = 0           ETA0      = 2.342963E-3     ETAB       = -1.5324E-4
+DSUB     = 0.0764123   PCLM      = 2.5941582       PDIBLC1    = 0.8187825
+PDIBLC2  = 2.366707E-3 PDIBLCB   = -0.0431505      DROUT      = 0.9919348
+PSCBE1   = 6.611774E8  PSCBE2    = 3.238266E-4     PVAG       = 0
+DELTA    = 0.01        RSH       = 83.5            MOBMOD     = 1
 +PRT      = 0           UTE       = -1.5            KT1        = -0.11
 +KT1L     = 0           KT2       = 0.022           UA1        = 4.31E-9
 +UB1      = -7.61E-18   UC1       = -5.6E-11        AT         = 3.3E4
 +WL       = 0           WLN       = 1               WW         = 0
 +WWN      = 1           WWL       = 0               LL         = 0
 +LLN      = 1           LW        = 0               LWN        = 1
 +LWL      = 0           CAPMOD    = 2               XPART      = 0.5
 +CGDO     = 2.32E-10    CGSO      = 2.32E-10        CGBO       = 1E-9
 +CJ       = 4.282017E-4 PB        = 0.9317787       MJ         = 0.4495867
 +CJSW     = 3.034055E-10 PBSW     = 0.8             MJSW       = 0.1713852
 +CJSWG    = 1.64E-10    PBSWG     = 0.8             MJSWG      = 0.1713852
 +CF       = 0           PVTH0     = 0.0520855       PRDSW      = 112.8875816
 +PK2      = -0.0289036  WKETA     = -0.0237483      LKETA      = 1.728324E-3   )
 *
```
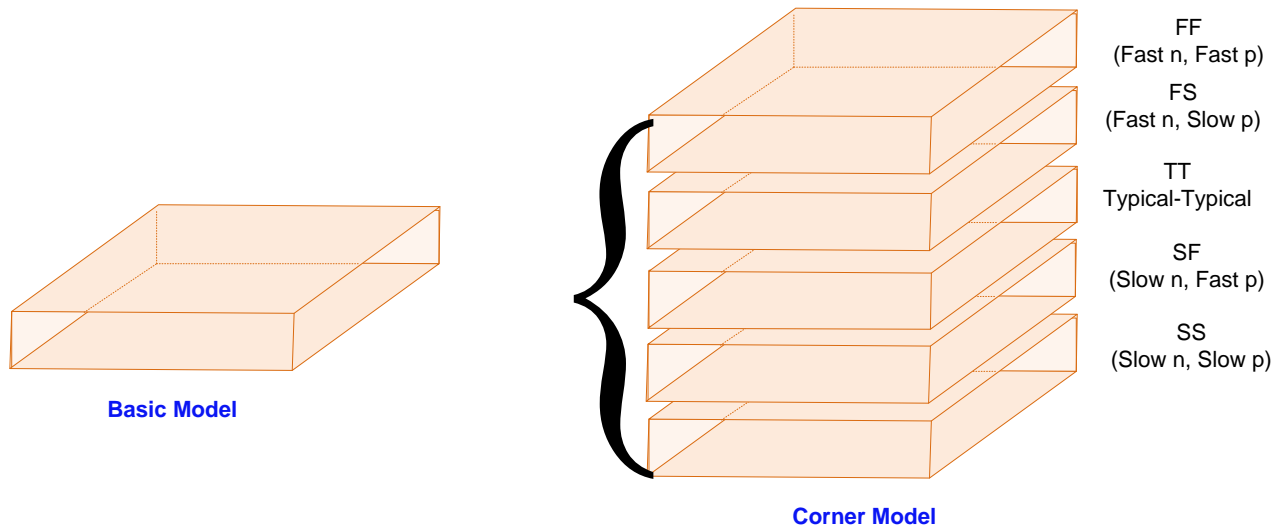
TT: typical-typical
FF: fast n, fast p
FS: fast n, slow p
SF: slow n, fast p
SS: slow n, slow p

With 4 corners, this model has 475 model parameters !

Hierarchical Model Comparisons

Accuracy
Complexity

Numerical (for simulation only)

Analytical

L

W

BSIM Binning
Models

Number of Model
Parameters

**Approx 3000
(for 30 bins)**

BSIM
Models

Number of Model
Parameters

Approx 100

Square-Law
Models

Number of Model
Parameters

3 to 6

Switch-Level
Models

Number of Model
Parameters

0 to 2

Corner Models

Basic Model

FF
(Fast n, Fast p)

FS
(Fast n, Slow p)

TT
Typical-Typical

SF
(Slow n, Fast p)

SS
(Slow n, Slow p)

Corner Model

Applicable at any level in model hierarchy (same model, different parameters)

Often 4 corners (FF, FS, SF, SS) used but sometimes many more

Designers must provide enough robustness so good yield at all corners

n-channel …. p-channel modeling
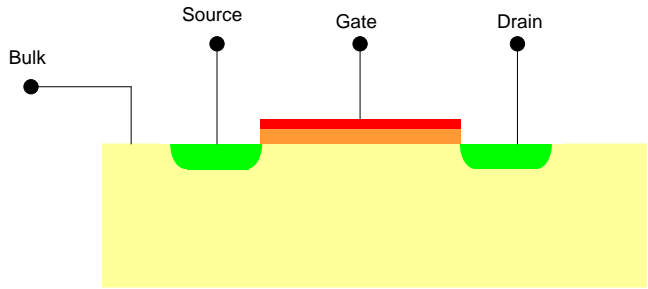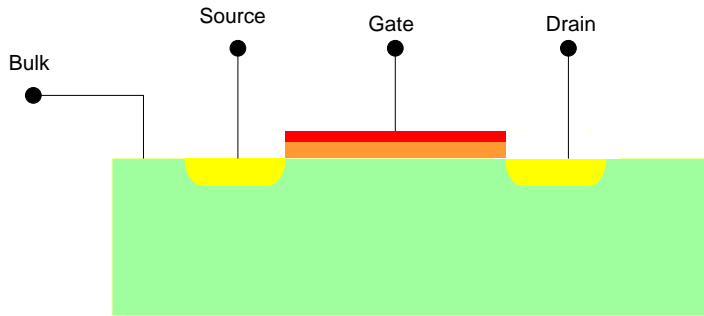

n-channel MOSFET
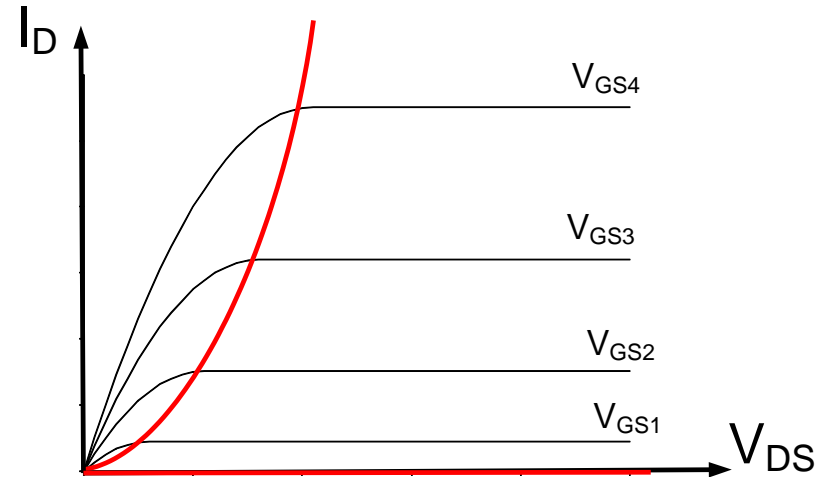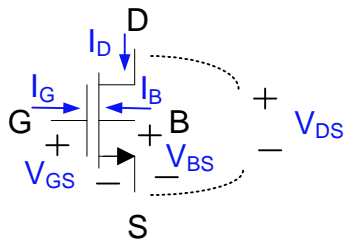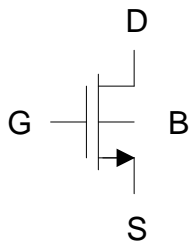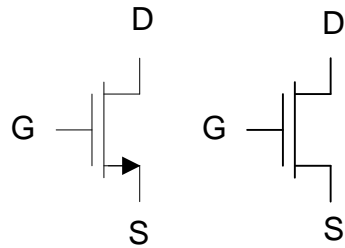
$V_{GS4} > V_{GS3} > V_{GS2} > V_{GS1} > 0$

(for enhancement devices)

$$I_D = \begin{cases} 0 & V_{GS} \le V_{Tn} \\[2mm] \mu_n C_{OX} \dfrac{W}{L}\left(V_{GS} - V_{Tn} - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_{Tn} \quad V_{DS} < V_{GS} - V_{Tn} \\[2mm] \mu_n C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_{Tn}\right)^2 & V_{GS} \ge V_{Tn} \quad V_{DS} \ge V_{GS} - V_{Tn} \end{cases}$$

$I_G = I_B = 0$

Positive V_{DS} and V_{GS} cause a positive I_D
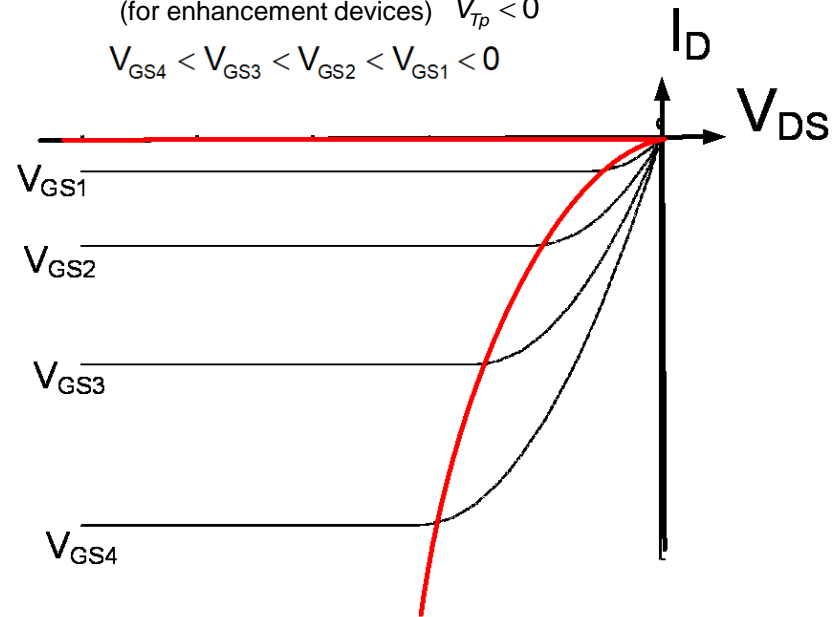
n-channel .... p-channel modeling

Source Gate Drain

Bulk

p-channel MOSFET
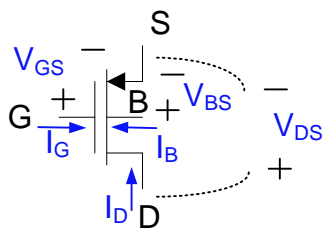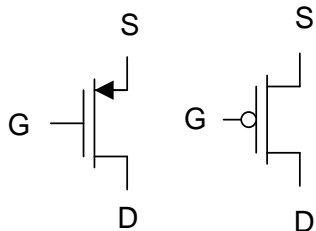
(for enhancement devices) $V_{Tp} < 0$

$V_{GS4} < V_{GS3} < V_{GS2} < V_{GS1} < 0$

I_D

V_{DS}

V_{GS1}

V_{GS2}

V_{GS3}

V_{GS4}

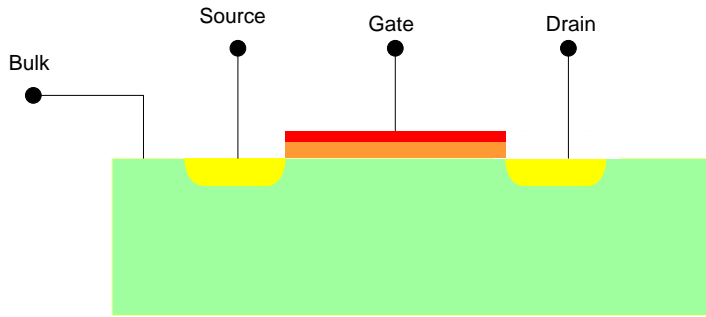V_{GS} S

G B V_{BS} V_{DS}

I_G I_B

I_D D

$$I_D = \begin{cases} 0 & V_{GS} \geq V_{Tp} \\ -\mu_p C_{OX} \dfrac{W}{L}\left(V_{GS} - V_{Tp} - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \leq V_{Tp} \quad V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_{Tp}\right)^2 & V_{GS} \leq V_{Tp} \quad V_{DS} \leq V_{GS} - V_{Tp} \end{cases}$$
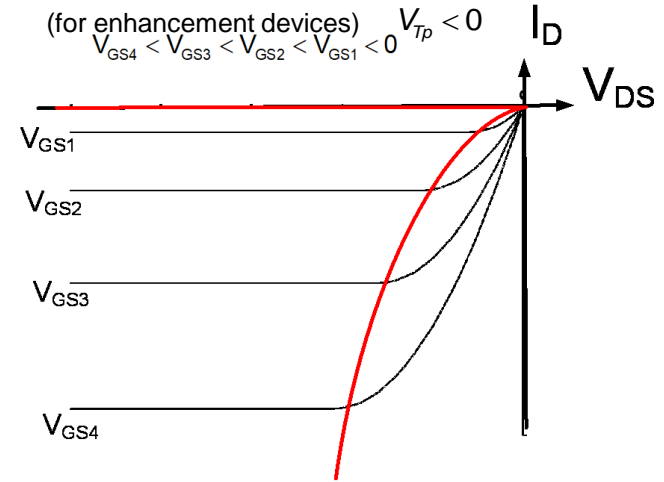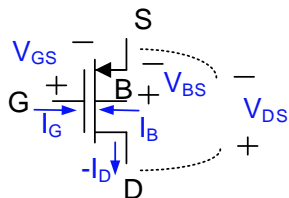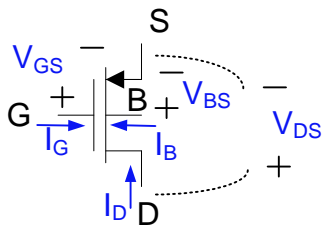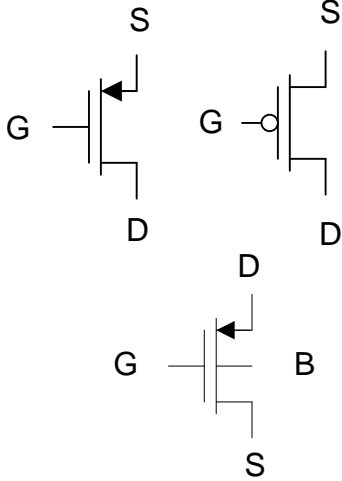
$I_G = I_B = 0$

Negative V_{DS} and V_{GS} cause a negative I_D

Functional form of models are the same, just sign differences and some parameter differences (usually mobility is the most important)

n-channel …. p-channel modeling

Source Gate Drain

Bulk

p-channel MOSFET

(for enhancement devices) $V_{Tp} < 0$ I_D
$V_{GS4} < V_{GS3} < V_{GS2} < V_{GS1} < 0$

V_{DS}

V_{GS1}

V_{GS2}

V_{GS3}

V_{GS4}

$$I_D = \begin{cases} 0 & V_{GS} \geq V_{Tp} \\ -\mu_p C_{OX} \dfrac{W}{L}\left(V_{GS} - V_{Tp} - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \leq V_{Tp} \quad V_{DS} > V_{GS} - V_{Tp} \\ -\mu_p C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_{Tp}\right)^2 & V_{GS} \leq V_{Tp} \quad V_{DS} \leq V_{GS} - V_{Tp} \end{cases}$$

$I_G = I_B = 0$

- Actually should use C_{OXp} and C_{OXn} but they are usually almost identical in most processes
- $\mu_n \approx 3\mu_p$
- May choose to model $-I_D$ which will be non-negative

Stay Safe and Stay Healthy !

End of Lecture 17